Secure Hash Algorithm (SHA)

- SHA was originally designed by the National Institute of Standards and Technology (NIST) and published as a federal information processing standard (FIPS 180) in 1993
- Was revised in 1995 as SHA-1
- Based on the hash function MD4 and its design closely models MD4
- Produces 160-bit hash values
- In 2002 NIST produced a revised version of the standard that defined three new versions of SHA with hash value lengths of 256, 384, and 512
 - Collectively known as SHA-2

Table 11.3 Comparison of SHA Parameters

	SHA-1	SHA-224	SHA-256	SHA-384	SHA-512
Message Digest Size	160	224	256	384	512
Message Size	< 2 ⁶⁴	< 2 ⁶⁴	< 2 ⁶⁴	< 2 ¹²⁸	< 2 ¹²⁸
Block Size	512	512	512	1024	1024
Word Size	32	32	32	64	64
Number of Steps	80	64	64	80	80

Note: All sizes are measured in bits.

SHA – 512 Processing Steps

- Step 1: Append padding bits. The message is padded so that its length is congruent to 896 modulo 1024 [length K 896(mod 1024)].
- Step 2: Append length. A block of 128 bits is appended to the message. The outcome of the first two steps yields a message that is an integer multiple of 1024 bits in length. I.e. every block is 1024 and last block also 896+128 bits = 1024 bits block
- Step 3 Initialize hash buffer. A 512-bit buffer is used to hold intermediate and final results of the hash function. The buffer can be represented as eight 64-bit registers (a, b, c, d, e, f, g, h)
- Step 4 Process message in 1024-bit (128-word) blocks. The heart of the algorithm is a module that consists of 80 rounds; this module is labelled F in Figure 11.9 The logic is illustrated in Figure 11.10.
- Step 5 Output. After all N 1024-bit blocks have been processed, the output from the Nth stage is the 512-bit message digest.



= word-by-word addition mod 2⁶⁴

Figure 11.9 Message Digest Generation Using SHA-512



Figure 11.10 SHA-512 Processing of a Single 1024-Bit Block

SHA-512 Logic

(Figure can be found on page 337 in textbook)

The padded message consists blocks $M_1, M_2, \dots M_N$. Each message block M_i consists of 16 64-					
bit words M _{i,0} , M _{i,1} M _{i,15} . All addition is performed modulo 2 ⁶⁴ .					
$H_{0,0} = 6A09E667F3BCC908$	$H_{0,4} = 510E527FADE682D1$				
$H_{0,1} = BB67AE8584CAA73B$	$H_{0.5} = 9B05688C2B3E6C1F$				
$H_{0,2} = 3C6EF372FE94F82B$	$H_{0.6} = 1F83D9ABFB41BD6B$				
$H_{0,3} = A54FF53A5F1D36F1$	$H_{0,7} = 5BE0CDI9137E2179$				
for $i = 1$ to N					
 Prepare the message schedule W: for t = 0 to 15 					
W = M					
for $t = 16$ to 79					
$W = \sigma_{s}^{512}(W_{s}) + W_{s} + \sigma_{s}^{512}(W_{s})$	()+W				
 Initialize the working variables 	1-15 / + 17-16				
$a = H_{i,1,0}$ $e = H_{i,1,4}$					
$b = H_{i_1,i_2} \qquad f = H_{i_1,i_2}$					
$c = H_{i_1 i_2}$ $g = H_{i_1 i_2}$					
$d = H_{1,1,2}$ $h = H_{1,1,2}$					
 Perform the main hash computation 					
for $t = 0$ to 79					
$T_1 = h + Ch(e, f, g) + \left(\sum_{1}^{512} e\right)$	$+ W_i + K_j$				
$T_2 = \left(\sum_{n=0}^{512} a\right) + \operatorname{Maj}(a, b, c)$					
h = g					
g = f					
f = e					
$e = d + T_1$					
d = c					
c = b b = a					
$a = T_1 + T_2$					
4. Compute the inermediate hash value					
$H_{i,0} = a + H_{i-1,0}$ $H_{i,4} = e + H_{i-1,4}$					
$H_{i,1} = b + H_{i-1,1}$ $H_{i,5} = f + H_{i-1,1}$	5				
$H_{i,2} = c + H_{i-1,2}$ $H_{i,6} = g + H_{i,1}$	6				
$H_{i,2} = d + H_{i,-1,2}$ $H_{i,2} = h + H_{i,-1,2}$	7				
return $\{H_{N,0} \parallel H_{N,1} \parallel H_{N,2} \parallel H_{N,3} \parallel H_{N,4} \parallel H_{N,5} \parallel H_{N,6} \parallel H_{N,7}\}$					

Figure 11.13 SHA-512 Logic